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Remarks

Thorough examination by the Examiner is noted and appreciated.

Support for the amended claims is found in the previously presented claims, the Specification and the Figures.

No new matter has been added.

For example support for the amendments and new claims is found in the original and previously presented claims as well as the Figures including Figure 1E:

Claim Objections

Claims 45, 47, and 49 have been amended to overcome Examiners objections.

Claim Rejections under 35 USC 103

1. Claims 18-22, 24, 25, 27-30, 32-35, and 38-50 stand rejected under 35 USC Section 103(a) as being unpatentable over Tamaru (US 2003/0030146) in view of Chen et al. (6,784,096).

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Tamaru disclose a **single contact layer** (16) with contact interconnect structures (18; e.g., Figures 6, 7) penetrating the single contact layer (16). Tamaru clearly disclose forming contact holes (**openings**) (17) in the single contact layer (16) and forming metal W plugs (18) (TiN barrier layer and W metal plug in the contact holes (paragraph 0079). Tamaru then disclose forming **wiring grooves (lines)** for forming **first layer Cu wiring** (24) (also known in the art to one of ordinary skill as a **metallization layer** (as opposed to a **contact openings in a contact layer**) including a "high melting metal nitride" barrier layer (TiN, Ti/TiN, WN, TaN, and Ta/TaN paragraph 0088) separating the **contact metal plugs** and the **Cu wiring in the metallization layer above the contact layer** (16) (see paragraphs 0080, 0087, 0088; Figures 6 and 7). Thus, in cross section the **Cu wiring** (24) overlies the **single contact layer including a contact interconnect structure i.e., contact plugs (metal filled holes)** (18) (see also Abstract and claim 1).

Therefore Tamaru fails to disclose Applicants invention including those elements in **bold type**:

With respect to claim 18:

"A **contact interconnect structure** comprising:

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a semiconductor substrate comprising CMOS devices including active contact regions;

a first contact layer overlying the active contact regions comprising a first plurality of metal filled contact openings extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second plurality of metal filled contact openings, each of said second plurality of metal filled contact openings extending through the second contact layer thickness to physically contact a major metal filling portion of a respective one or more of the first plurality of metal contact filled openings;

wherein, the first plurality and the second plurality of metal filled contact openings **form a physically continuous contact interconnect structure**, said first and second metal filled contact openings having an aspect ratio of less than about 4.5 with respect to a respective contact layer, **said contact interconnect structure connecting said active contact regions to overlying wiring circuitry comprising metallization layers."**

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With respect to claim 32:

"A contact interconnect structure comprising:

at least first and **second stacked contact layers** comprising a respective first and second plurality of **metal filled contact openings**, extending through the respective first and second contact layers to a contact region comprising an active transistor region, **said first and second plurality of metal filled contact openings forming physically contacting major metal filling portions comprising said stacked contact interconnect structure;**

wherein, the first plurality and the second plurality of metal filled contact openings comprise a **bottom portion having a maximum width of less than about 70 nanometers**, said first and second metal filled contact openings having an aspect ratio of less than about 3.3 with respect to a respective contact layer, said contact interconnect structure connecting said active contact regions to overlying wiring circuitry comprising metallization layers.

With respect to claim 38:

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"A stacked contact interconnect structure for achieving a high aspect ratio comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first contact layer overlying the active contact regions comprising a first metal filled contact opening extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second metal filled contact opening extending through the second contact layer thickness to physically contact a major metal filling portion of the first metal filled opening;

wherein, each of the first and second metal filled contact openings have about the same width to form a physically connected stacked contact interconnect structure, said first and second metal filled contact openings having an aspect ratio of less than about 4.5 with respect to a respective contact layer, said contact interconnect structure connecting said active contact regions to overlying wiring circuitry comprising metallization layers."

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Thus, one of ordinary skill would understand that **the metallization layers including wiring structures** of Tamaru (as taught by Tamaru) are **different structures** than the **contact plugs (contact interconnect structures - metal filled holes)** of Tamaru formed in a **single contact layer** (i.e., one of ordinary skill would understand the plain meaning and the difference of structure and function of contact interconnect structures (contact plugs) in a contact layer versus wiring structures in a metallization layer as taught by Tamaru.

See e.g., MPEP 2111.01:

During examination, the claims must be interpreted as broadly as their terms reasonably allow. **This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification.** *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

When not defined by applicant in the specification, **the words of a claim must be given their plain meaning. In other words, they must be read as they would be interpreted by those of ordinary skill in the art.** *In re Sneed*, 710 F.2d 1544, 218 USPQ 385 (Fed. Cir. 1983).

Examiner is erroneously (and contrary to the understanding of the structures and plain meaning of Applicants claim language to one of ordinary skill and as is further evidenced by the

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teachings of Tamaru itself) equating the metallization layer (including wiring grooves) of Tamaru as equivalent to Applicants second contact layer (including the contact interconnect structure).

Moreover, as noted above, Tamaru nowhere discloses or suggests that the Cu filled wiring grooves **physically contact** a major metal filling portion of the metal filled (W) contact plugs (i.e., tungsten). Rather Tamaru clearly disclose **a metal nitride barrier layer between the two major metal filling portions of the structures** (see paragraphs 0080, 0087, 0088; Figures 6 and 7).

In contrast to Tamaru, and in non-analogous art, Chen et al. disclose a method of **forming a barrier layer to line vias** where the **vias** are disclosed to have a width less than 70 nm or an aspect ratio greater than about 3:1 (see Abstract; Figures).

"Embodiments of the present invention provide **methods and apparatus for forming barrier layers in high aspect ratio vias (e.g., vias having aspect ratios of 3:1, 4:1, 5:1 or higher) and/or vias having via widths of about 0.065-0.2 microns or below**. It will be understood that the invention also may be employed to form barrier layers in lower aspect ratio and/or wider vias. Each embodiment allows a relatively thick barrier layer to be deposited on the sidewalls of a via with little or no barrier layer coverage on the bottom of the via. Adequate diffusion resistance and/or mechanical strength thereby may be provided without significantly increasing the contact resistance of the interconnect formed with the via."

Even assuming *arguendo*, a proper motivation to modify Tamaru

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based on the teachings of Chen et al., such modification **fails to produce Applicants invention.**

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).

With respect to claims 46, 48, and 50 Examiner is mistaken that Tamaru discloses that the first and second plurality of metal filled contact openings are connected to one another. As

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noted above, Tamaru nowhere discloses metal filled contact openings contacting one another but rather discloses Cu wiring in a metallization layer contacting a **metal nitride barrier layer** formed between contact plugs and the wiring.

Therefore Tamaru clearly further fails to disclose a metal filled contact interconnect structures **physically contacting one another.**

With respect to claims 47, and 49 Examiner is mistaken that Tamaru discloses "The contact interconnect structure of claim 38, wherein the first plurality and the second plurality of metal filled contact openings comprise the same material."

Rather, as noted above, Tamaru discloses Cu wiring and nowhere discloses Cu contact plugs, and further discloses a metal nitride barrier layer between the Cu wiring and the W contact plugs.

2. Claims 26 and 36 stand rejected under 35 USC Section 103(a) as being unpatentable over Tamura, above in view of Chen et al., above, and further in view of Ono (IEE Trans on Electronic Devices, pg 1822 Vol. 42, No. 10, 1995).

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Applicants reiterate the comments made above with respect to Tamura and Chen et al.

Even assuming *arguendo*, a proper motivation to further modify Tamura with the teachings of Ono, the further fact that Ono discloses a gate length of less than about 45 nm without a corresponding disclosure or teaching of a contact interconnect structure does not further help Examiner in producing Applicants invention.

"**First**, there must be some **suggestion or motivation**, either, in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

"The fact that references relied upon teach that all aspects of the claimed invention were individually known in the art is

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not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

Examiners Arguments

Applicants have stated the fact that Tamaru discloses a **metallization layer with wiring grooves (lines) overlying a single contact layer with contact plugs (holes)**. Examiner has erroneously and contrary to the **plain meaning** of the language 'contact layer' and 'contact interconnect structures' as would be understood by one of ordinary skill in that art as further evidenced by the teachings of Tamaru, attempted to equate the metallization layer and wiring grooves of Tamaru with Applicants second contact layer and contact interconnect structures.

Examiner has responded that "The arguments that Tamaru does not teach the claimed contact interconnect structure and contact openings are not persuasive. **Neither the claim language nor the record precludes** reading the claims onto the structure of Tamaru".

Thus, Examiner simply ignores the plain meaning of

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Applicants claim language as would be understood by one of ordinary skill in the art as is further evidenced by the teachings of the cited art itself, Tamaru. Examiner gives no guidance at all as to his reasoning or how he can cite Tamaru as a reference yet ignore the difference in the structures "wiring groove" in a metallization layer and a contact interconnect structure in a contact layer as is evidenced by the teachings of Tamaru itself. Further, it is not understood what Examiner means by referring to the **record** or how the record **does not preclude** reading the claims onto the structure of Tamaru.

It is not the burden of Applicants to preclude Examiner from misinterpreting a reference, rather the burden is on Examiner to make out a *prima facie* case of obviousness (**Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**) as defined by both the Patent Office and the Courts, while giving Applicant claim language its **plain meaning** as would be understood by one of ordinary skill in the art.

Examiner cites no support for his position (of simply deeming the wiring grooves and metallization layer of Tamaru are equivalent to Applicants contact interconnect structures contrary to the teachings of Tamaru), nor gives any guidance as to his

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reasoning. The further statement that Applicants are somehow being bound by the record of prosecution is not explained and does not comport with any standard of determination for obviousness as established **by the Patent Office or the Courts.**

For example, it appears that Examiner is apparently attempting to argue that Applicants amendments to clearly define over the prior art as somehow objectionable or not permitted. Applicants are left to guess at Examiners reasoning as to how Examiner can ignore the plain meaning of both the cited references and Applicants claim language or what portion of the record Examiner is relying on to prevent Applicants from amending their claims to define over the prior art, thus preventing the goal of examination; to **define a clear issue between Examiner and Applicant** "To bring the prosecution to as speedy conclusion as possible and **at the same time to deal justly with both the applicant and the public**". Examiner is referred to the following portion of the MPEP establishing binding guidance for examination of Patent Applications.

MPEP 706.07

Before final rejection is in order a clear issue should be developed between the examiner and applicant.
To bring the prosecution to as speedy conclusion as possible and at the same time to deal justly by both the applicant and the public, the invention as disclosed and claimed should be thoroughly searched in the first action and the references fully applied; and in

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reply to this action the applicant should amend with a view to avoiding all the grounds of rejection and objection. Switching from one subject matter to another in the claims presented by applicant in successive amendments, or from one set of references to another by the examiner in rejecting in successive actions claims of substantially the same subject matter, will alike tend to defeat attaining the goal of reaching a clearly defined issue for an early termination, i.e., either an allowance of the application or a final rejection.

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

"The initial burden is on the examiner to provide some suggestion of the desirability of **doing what the inventor has done**. "To support the conclusion that the claimed invention is directed to obvious subject matter, either **the references must expressly or impliedly suggest the claimed invention** or the

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examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

Obviousness can only be established by combining or modifying the teachings of the prior art **to produce the claimed invention** where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Applicants have nevertheless further amended their claims to even further define over the Cu metallization layer with wiring of Tamaru contacting a barrier layer on the contact plugs of Tamaru.

Conclusion

The cited references, singly or in combination fail to produce or suggest the elements of Applicants invention, and therefore fail to make out a *prima facie* case of obviousness.

Applicants have nevertheless, further amended their claims

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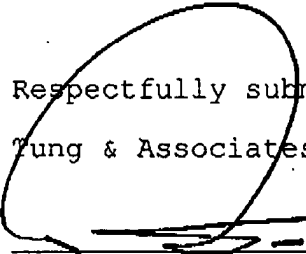
to further define over the prior art. Applicants respectfully request favorable reconsideration of their claims.

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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